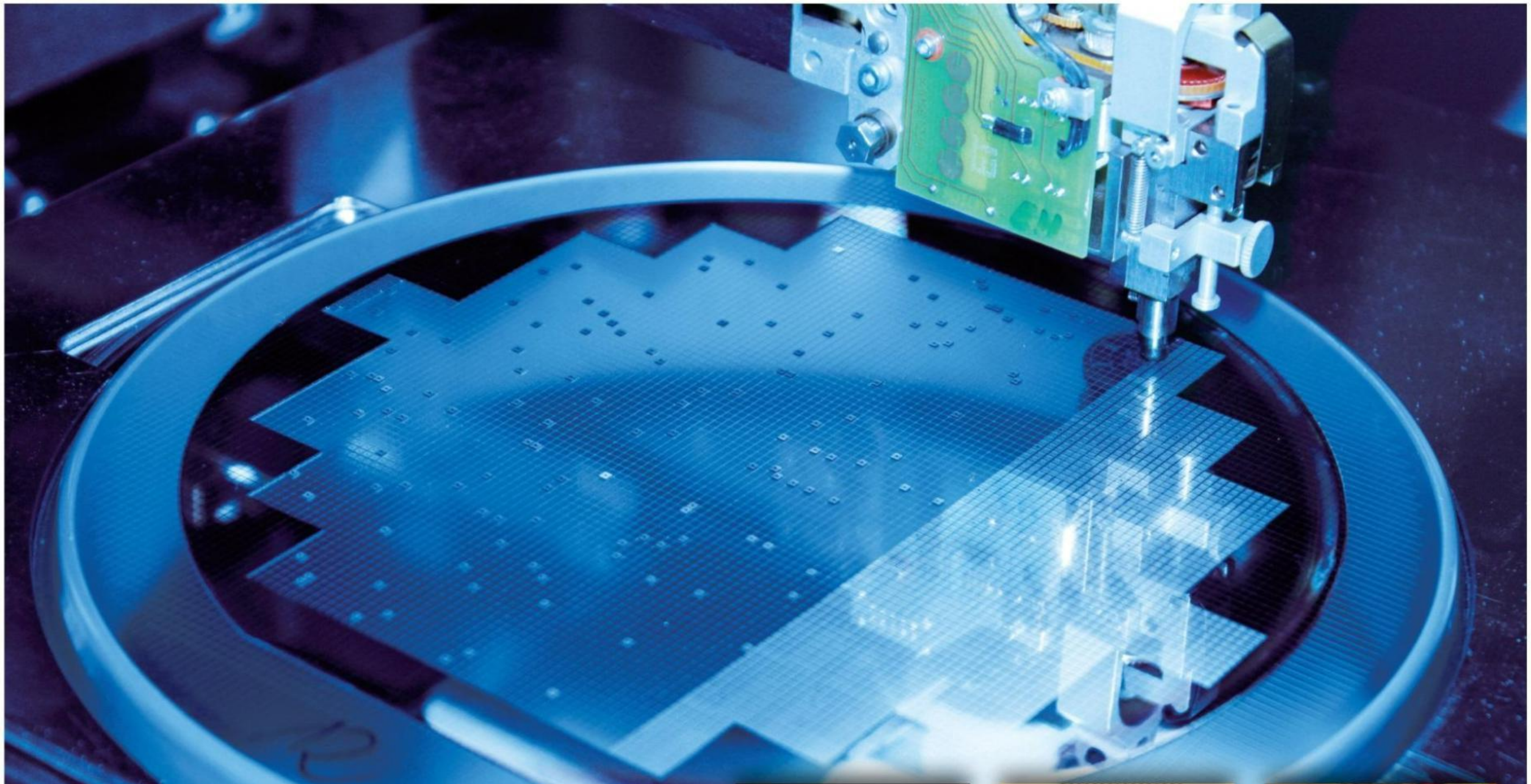
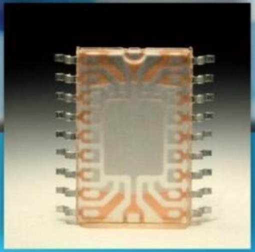
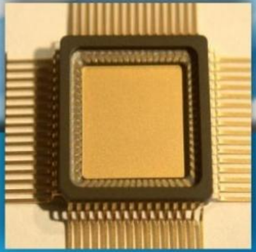
Packaging for electronic components „Made in Germany“







MAF
Microelectronic Assembly
Frankfurt (Oder) GmbH

History of the company

- 1998 founded by Dipl.-Ing. Michael Göpel
- East of Berlin, on the boarder with Poland
- Spin-off of the largest microelectronics manufacturer "HFO Halbleiterwerk" of the former GDR
- Since 2006 daughter company of the HTV group of companies

General Information

One of the few specialists for packaging and assembly of microelectronic circuits in Europe!

Production location: Otto-Hahn-Str. 24, 15236 Frankfurt (Oder), Germany

Production area :

- 220 qm, ESD protected area
- Temperature: 25 °C ± 2°C
- Humidity: 30 - 70 % relative air humidity

Product range:

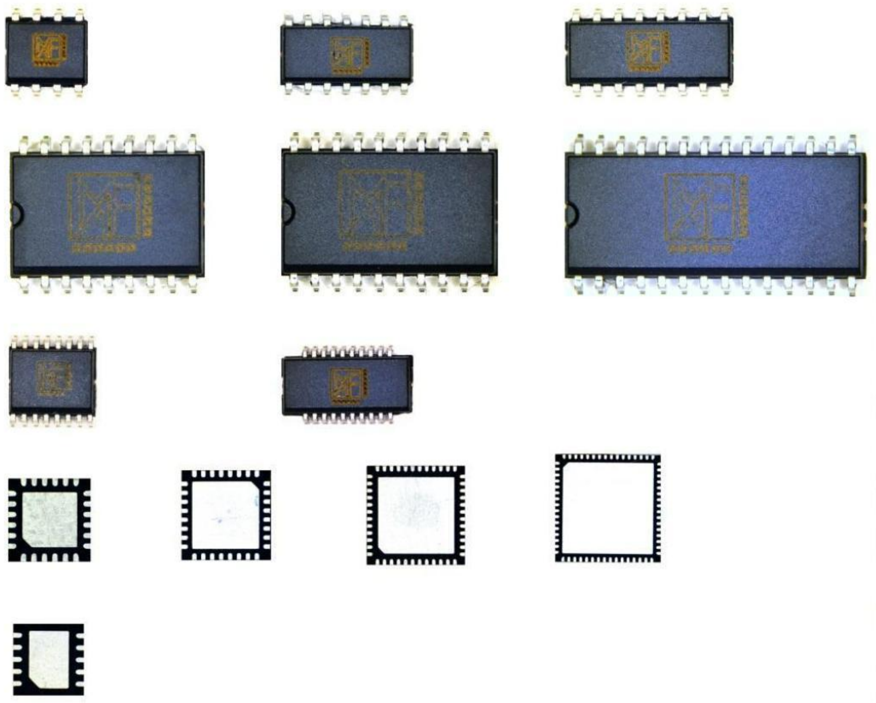
- Backside grinding (thinning)
- Wafer-dicing
- DIE sorting
- Plastic standard packages (such as SOP, SSOP, PQFP, QFN, DFN)
- Customised packages
- Samples assembly (ceramic, Premold)
- COB (Chip on Board)

Production capacity: approx. 15 million components

Main production - plastic packages

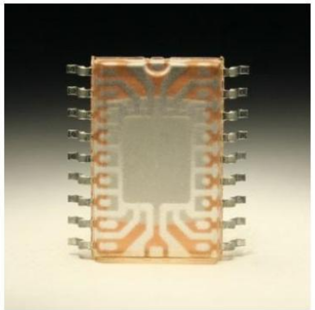
Standard packages:

- **JEDEC-MS-012, SOP**
  Pin 8/14/16
- **JEDEC-MS-013, SOP**
  Pin 18/20/28
- **JEDEC-MO-137, SSOP**
  Pin16/20
- **JEDEC-MO-220, QFN**
  Pin 24/32/48/64
- **JEDEC-MO-229, DFN**
  Pin 10

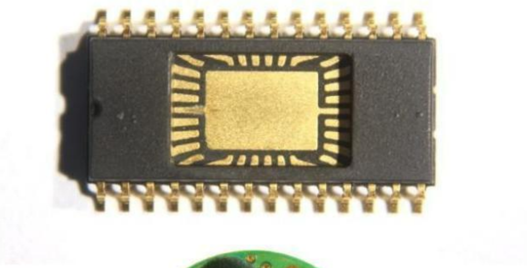


Customised packages according to customer requirements

- **customised packages for specific applications,**
  e.g. with several dies or in transparent packages

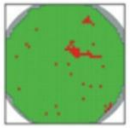


- Sample preparation in a **Premold or ceramic package** (open cavity)

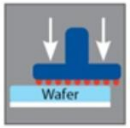


- **Chip-On-Board assembly**

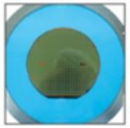
Packaging Process



Electronic
wafer map

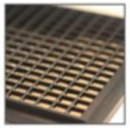


Backside grinding
(Thinning of the wafer)



Mounting of the
wafer on foil

Wafer dicing
sorting of failed parts



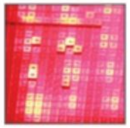
Pick&Place the chips
in waffle pack

Chip bonding
on leadframe

Fully automated
wire bonding
chips - leadframe

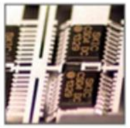
Quality control:
visual inspection/
Pull- and Shear test

Molding process/
overmoulding of the
leadframes with epoxy resin



Customer-specific marking of
the components, e.g. with laser

Tin plating of the leadframes



Trim & Form process:
bending and separating
of connections

Packing
(Tray, Tube, Tape and Reel)

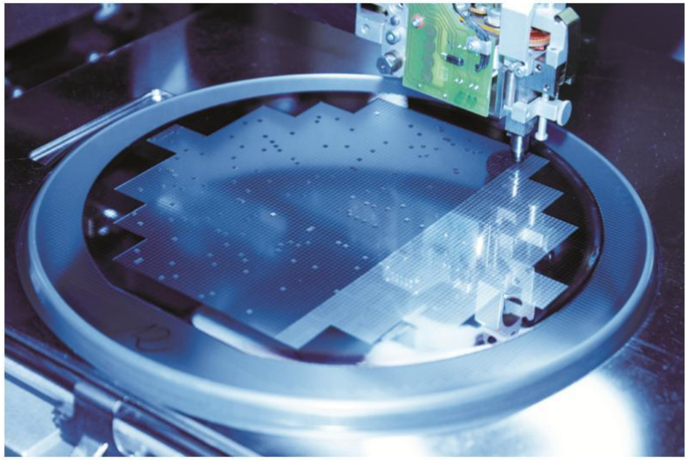
Wafer dicing

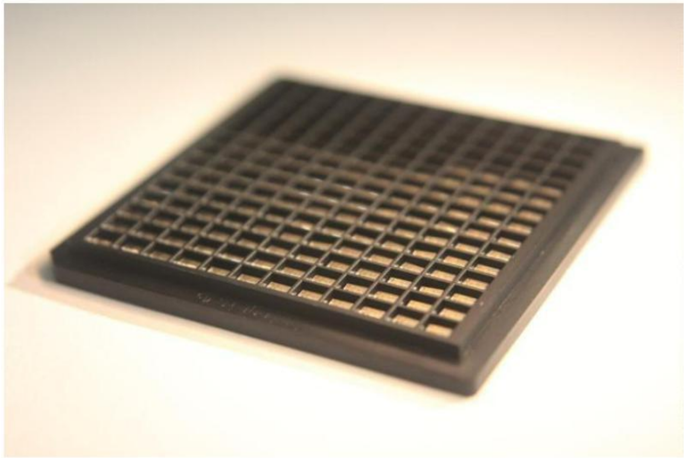
Dual spindle dicing saw DFD651

- Integrated washing station
- In-house 8” wafer dicing
- Si and SiGe

DIE-Sorting/Pick&Place

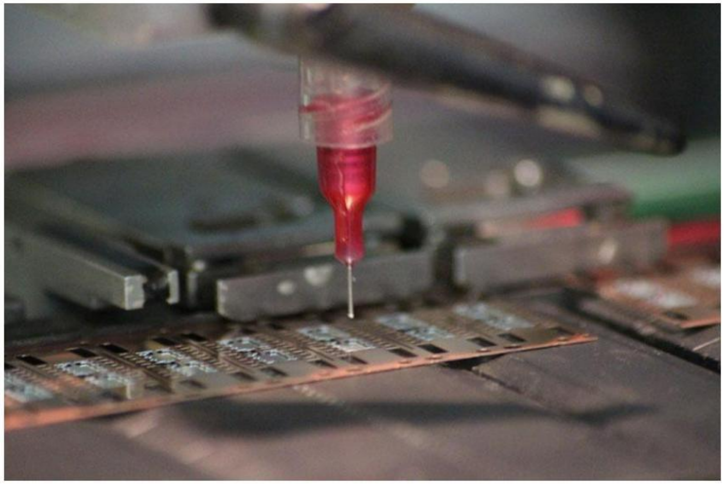
- DIE-Sorting in Waffle-Pack
(Standard- & Multiproject-Wafer)
- Fully automated DIE-Sorting
(DS3020 & ESEC 2008xP)
- Sorting in 2“/4“ Trays, JEDEC-Trays or Gel-Pack



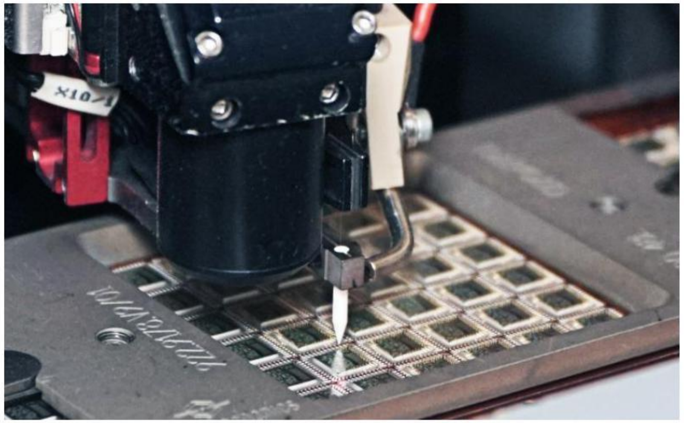


Chip bonding

- Fully automated chip bonding (Epoxy adhesive): ESEC 2008xP
- Processing of wafers up to 8'' possible
- Curing/Tempering of epoxy adhesive in the oven



Wire bonding

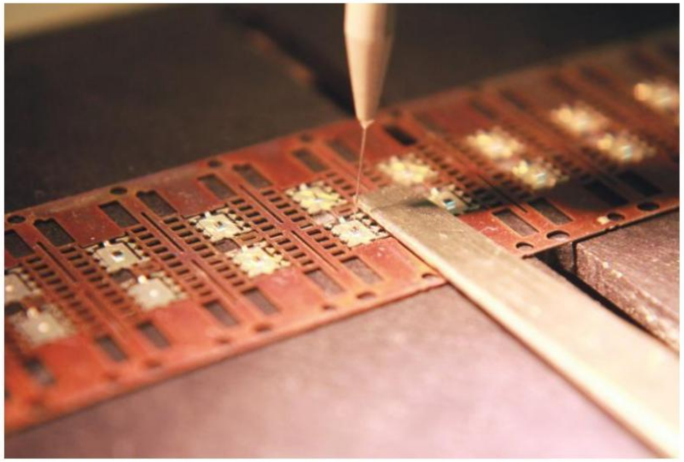


- Fully automatic Au-wire bonder ESEC 3088 & ESC 3006 F/X & ESEC 3200

  (Au-wire 25µm und 32µm)

- Carried out by means of thermocompression processes

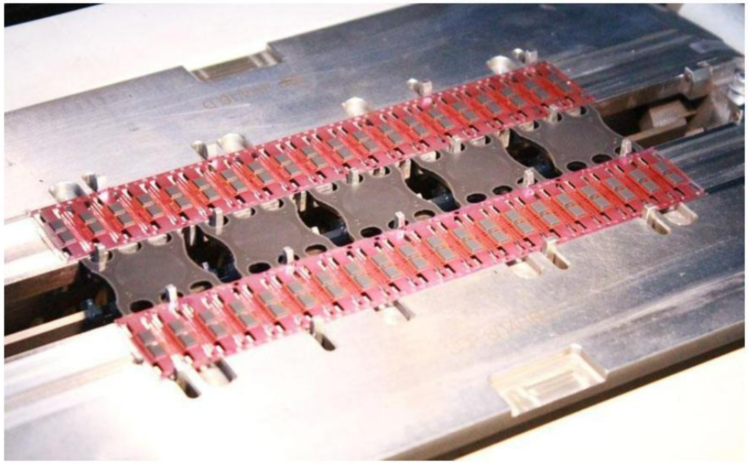
- Testing the bond quality with Pull- und Sheartest

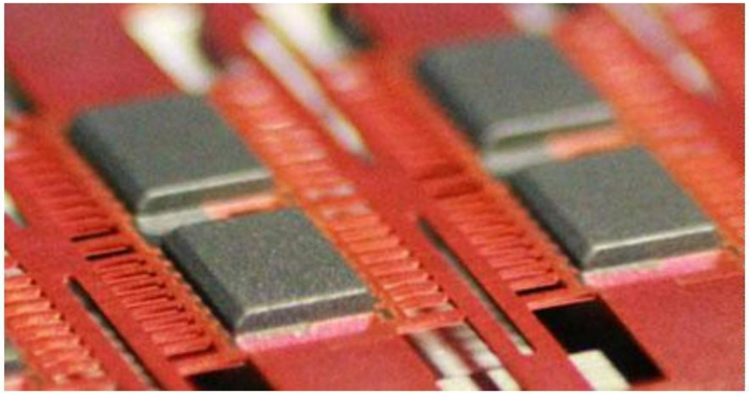


Molding

Fully automated moulding with AMS 12/24 M multi plunger

- Molding with epoxy resin (MP8000 or GE7470)
- Minimal effort for product modifications





Labeling

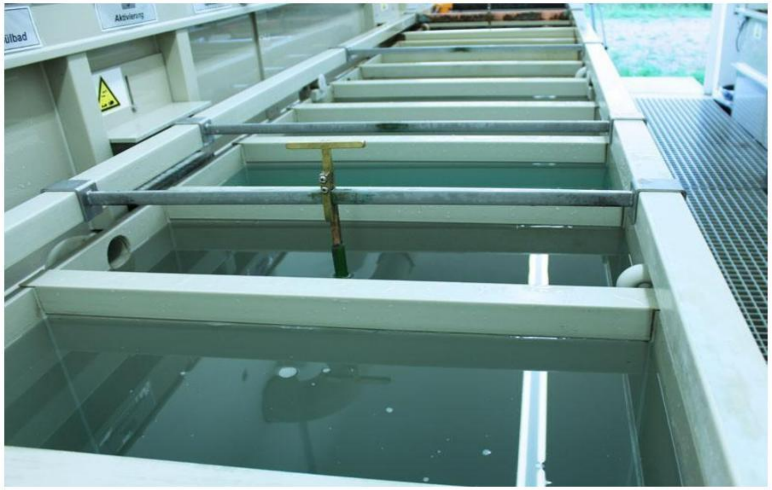
- Laser station with the dambar cutting

- Yb-Fiber-Laser very flexible & fast programmable

- Marking by customer requirements

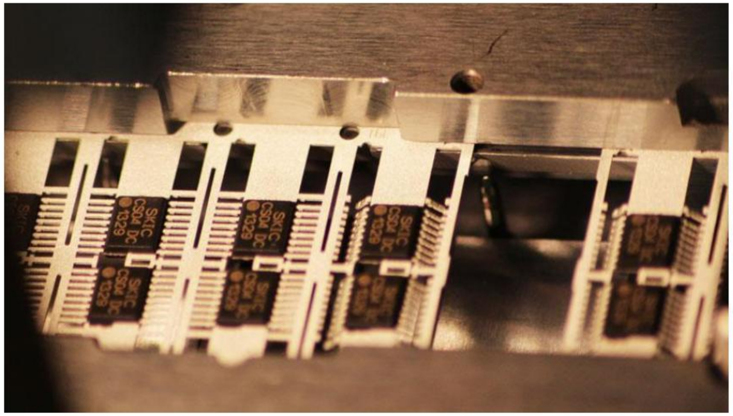
Tinning

- Tinning on the rack
- 100% lead-free matt tin
- Checking the tin quality with soldering and bending test



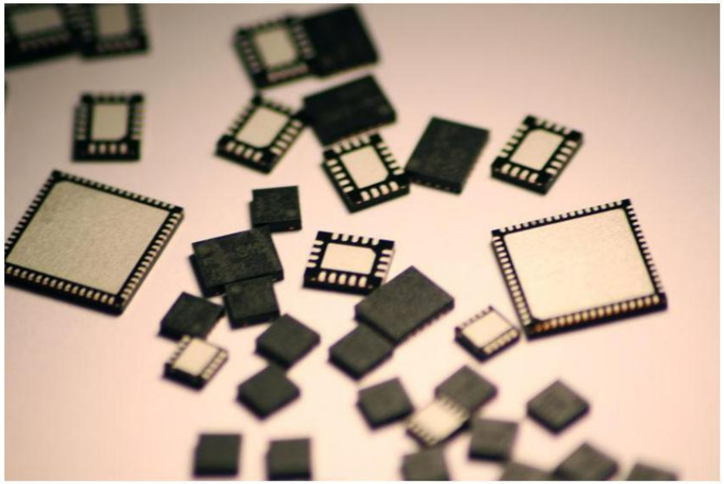
Trim & Form of SOxxx/PQFP

- Fully automated forming on M-Press and on FPS 6000
- Automatic reloading
- Automatic packing in tubes (SOxxx) or trays (PQFP).




Separation of QFN/DFN

- Fully automated separation with ProDice ADT
- Integrated washing station
- Packing is carried out in JEDEC trays or tubes



Professional and complete service at the highest level

Preparation

Electronic wafer map

Backside grinding (Thinning of the wafer)

Chips separation

Mounting of the wafer on foil

Wafer dicing sorting of failed parts

Pick&Place the chips in waffle pack

Chips mounting

Chip bonding on leadframe

Fully automated wire bonding chips - leadframe

Quality control: visual inspection/ Pull- and Shear test

Encapsulation of chips

Standard packages
(such as SOP, SSOP, PQFP, QFN, DFN)

Quality control: visual inspection/ Pull- and Shear test

Molding process/ overmoulding of the leadframes with epoxy resin

Customer-specific marking of the components, e.g. with laser

Tin plating of the leadframes

Trim & Form process: bending and separating of connections

Packing (Tray, Tube, Tape and Reel)

Customised packages

e.g. transparent packages

Sample preparation
(Premold or ceramic package)

Labeling

Covering (cover, Glop Top)

Chip on Board (COB)

DIE's bonding directly to a printed circuit board

Contact

„Together we develop the optimal Package made in Germany for your specific application !"

Thilo Tröller
Bachelor of Sales and Distribution
CEO

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ISO 9001
BUREAU VERITAS
Certification

Thank you

for your attention.